## Proton SEE Test Report for the ST 1G NAND Flash Memory

Tim Oldham/QSS Group, Inc./NASA-GSFC
Christian Poivey/Muniz Engineering/NASA-GSFC
Ray Ladbury/NASA-GSFC
Hak Kim/Muniz Engineering/NASA-GSFC
Mark Friendlich/Muniz Engineering/NASA-GSFC
Melanie Berg/ Muniz Engineering/NASA-GSFC

Test Date: 7/27/2006 Report Date: 12/15/2006

#### I. Introduction

This study was undertaken to determine the susceptibility of the STMicroelectronics NAND01GW3B2ANGE 1 Gbit NAND Flash memory to destructive and nondestructive single-event effects (SEE). The device was monitored for SEUs and for destructive events induced by exposing it to a proton beam at the Indiana University Cyclotron Facility (IUCF).

## II. Devices Tested

We tested a STMicroelectronics 1G NAND flash device, part number NAND01GW3B2ANGE, marked with date code 604. Although five parts were available, only one was actually tested, due to time limitations. Note that with commercial devices, the same lot date code is no guarantee that the devices are from the same wafer diffusion lot or even from the same fabrication facility. The device technology is 90 nm minimum feature size CMOS NAND Flash memory.

## III. Test Facility

Facility: IUCF

**Flux:**  $(4 \times 10^7 \text{ to } 8 \times 10^8 \text{ particles/cm}^2/\text{s}).$ 

Fluence: All tests were run to  $(2 \times 10^{11} \text{ p/cm}^2)$  or until destructive or functional events

occurred.

Table I: Ions/Energies and LET for this test

Ion/Energy	Approx. LET on die (MeV•cm²/mg)
Protons/100 MeV	.006
Protons/200 MeV	.0036

## **IV.** Test Conditions

**Test Temperature:** Room Temperature for SEU

**Operating Frequency:** (0-100 MHz).

**Power Supply Voltage:** (3.3V and 3.3V-10% for SEU).

#### V. Test Methods

Because Flash technology uses different voltages and circuitry depending on the operation being performed, testing was performed for a variety of test patterns and bias and operating conditions.

In general, test patterns can be all 0's, all 1's, checkerboard and inverse checkerboard. In general all these patterns will be used until a worst-case pattern was established, and then testing was conducted using only the worst-case pattern. In this test, only seven shots were actually conducted, but all the patterns were used, except the inverse checkerboard (55).

Bias and operating conditions included:

- 1) Static/Unbiased irradiation, in which a pattern was written and verified, and then bias was removed from the part and the part was irradiated. Once the irradiation reached the desired fluence, it was stopped, bias was restored, and the memory contents were read and errors tallied.
- 2) Static irradiation, which was similar to unbiased irradiation, except that bias was maintained throughout irradiation of the part.

Note that these conditions provide no opportunity to monitor functional or hard failures that may occur during the irradiation.

- 3) Dynamic Read, in which a pattern was written to memory and verified, then subsequently read continuously during irradiation. This condition allows determination of functional, configuration and hard errors, as well as bit errors.
- 4) Dynamic Read/Write, which was similar to the Dynamic Read, except that a write operation is performed on each word found to be in error during the previous Read.
- Dynamic Read/Erase/Write, which again was similar to the Dynamic Read and Read/Write, except that a word in error was first erased and then rewritten. Because the Erase uses the charge pump, it is expected that the Flash could be more vulnerable to destructive conditions during this operation.

The Block diagram for control of the DUT is shown in Figure 1. The FPGA based controller interfaces to the FLASH daughter card and to a laptop, allowing control of the FPGA and uploading of new FPGA configurations and instructions for control of the DUT. Power for the FLASH is supplied by means of a computer-controlled power supply. The National Instruments Labview interface monitors the power supply for overcurrent conditions and shuts down power to the DUT if such conditions are detected.

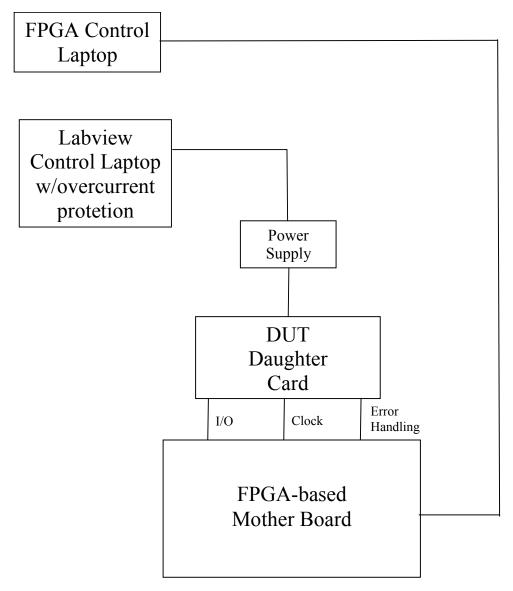


Figure 1. Overall Block Diagram for the testing of the ST NAND Flash.

#### VI. Results

During testing, the NAND01GW3B2ANGE was irradiated with protons, at 200 MeV, with results indicated in Table II below. All the exposures were done at normal incidence. There were no static errors observed in any of tests, indicating that the individual bits were not flipped by the proton interactions. In shot no. 2, a dynamic read test with a checkerboard pattern, small number of errors was observed with the beam on, but after the exposure, the bits had not been altered. This means there were erroneous reads, due to something in the peripheral circuits. Two other dynamic read tests were conducted on shots no. 6 and 7, with all zeroes and all ones stored, respectively. These shots produced nearly the same number of errors. But, ones-to-zero errors are the wrong polarity to be attributed to radiation-induced positive charge, so this result is clearly due to some problem in the peripheral circuits. There were two shots in the dynamic

read/write mode. The first of these had six bit errors recorded with the beam on, and seven errors when the DUT was checked again after the exposure. The second of these shots was interrupted, because of a latchup, the only one recorded for this part. There was also one shot in the read/erase/write dynamic mode, with all zeroes stored, where 27 errors were recorded. Cross sections are generally in the range from one to a few times  $10^{-10}$  cm<sup>2</sup> per device. Error cross sections per bit would be another nine orders of magnitude below this range.

There was no latchup observed in any of the exposures, but the testing was all done at room temperature, so this was not a worst-case test.

DUT DUT Quiescent SEL Proton SEL/ Cross SEOS SEL SEOS Time Temp TID Fluence Run# Component Mode Pattern Flux angle **DUT** current limit Errors Dest Energy Section sigma sigma 0.1 ST 1G FLASH 0.0033 Static AΑ 200 room 4.82E+03 0 0 0 508 8.37E+10 0 1.60E+08 Dynamic ST 1G FLASH 0.0033 200 4.82E+03 0 0 8.37E+10 5.00E+08 3.23E-10 AΑ room 27 144 read Dynamic 3^ ST 1G FLASH 0.0033 AA 200 room 4.03E+03 6 0 0 124.7 6.99E+10 5.00E+08 8.58E-11 Dynamic ST 1G FLASH 0.0033 200 1.32E+03 2.30E+10 5.90E+08 2.17E-10 R/W AA room 5 0 1 39.8 0 ST 1G FLASH 4.83E+03 27 0 5.40E+08 3.22E-10 0.0033 0.1 R/E/W 00 200 0 155 8.39E+10 room Dynamic ST 1G FLASH 0.0033 Read 200 room 4.82E+03 24 0 0 147.7 8.37E+10 5.67E+08 2.87E-10 Dynamic

Table II. Proton test results for ST 1G NAND flash.

Read

FF

200

room

0.0033

ST 1G FLASH

#### VII. Recommendations

4.82E+03

145.9

8.37E+10

5.79E+08 2.63E-10

In general, devices are categorized based on test data into one of the four following categories:

- Category 1: Recommended for usage in all NASA/GSFC spaceflight applications.
- Category 2: Recommended for usage in NASA/GSFC spaceflight applications, but may require mitigation techniques.
- Category 3: Recommended for usage in some NASA/GSFC spaceflight applications, but requires extensive mitigation techniques or hard failure recovery mode
- Category 4: Not recommended for usage in any NASA/GSFC spaceflight applications. Research Test Vehicle: Please contact the P.I. before utilizing this device for spaceflight applications

The STMicroelectronics NAND01GW3B2ANGE 1 Gbit NAND Flash memory is a Category 3 device.

<sup>\* =</sup> No errors after run ended and part read back

<sup>^ = 7</sup> errors remained after beam stopped; fixed after rewrite

<sup>+ =</sup> Watchdog error

# VIII. Further Test Requirements

This test represents a preliminary characterization of SEE vulnerability of the Micron MT29F2G08B. Additional testing is required before these devices can be considered for space applications. These components have also been tested with heavy ions, with measurable effects of many different kinds. Effective mitigation strategies have not yet been worked out, but they will be necessary before use in space is possible. In prior TID testing, these devices showed some promise for applications with moderate dose levels. Additional TID testing is recommended to fully characterize TID degradation.